# ULTRA HIGH-SPEED SEMICONDUCTOR INTEGRATED CIRCUIT CHIP INTERCONNECT STRUCTURE AND FABRICATION METHOD USING FREE-SPACE DIELECTRICS

ABSTRACT OF THE INVENTION:

Ultra high-speed multi-level interconnect structure and fabrication process flows are disclosed for a semiconductor integrated circuit chip. The interconnect structures of this invention include a plurality of electrically conductive metallization levels. Each of the metallization levels includes a plurality of electrically conductive interconnect lines. A plurality of electrically conductive plugs make electrical connections between various metallization levels as well as between the metallization levels and the semiconductor devices fabricated on the semiconductor substrate. The invention further includes a free-space medium occupying at least a substantial fraction of the electrically insulating regions within the multi-level interconnect structure surrounding the interconnect lines and plugs. A top passivation overlayer hermetically seals the multi-level interconnect structure. The top passivation overlayer used for hermetic sealing also functions as a heat transfer medium to facilitate heat removal from the interconnect metallization structure as well as to provide additional mechanical support for the multi-level interconnect structure through contact with the top metallization level of the multi-level interconnect structure. The hermetically sealed free-space medium minimizes the capacitive cross-talk noise in the

interconnect structure, enabling increased chip operating speeds and reduced chip power distribution.